Status of power consumption study of FPGA correlators

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Overview

- Correlator under consideration for both near and far-side radio arrays
- How will power, mass, capability of correlator scale as a function of number of baselines, bandwidth, technology?
- Xilinx Virtex 5 FPGA selected for studies
  - May be flight-worthy in 5 years
  - Probably within factor of 10-100 of what we should expect within a decade without intense development effort
- Tour of test setup described in talk this afternoon
Collaboration for Astronomy Signal Processing and Electronics Research

Mission: to reduce design cycle time of astronomy back ends

Uses platform independent open source software and hardware (FPGA, GPU, CPU)

CASPER workshop at CfA 16-20 August 2010

http://casper.berkeley.edu
CASPER design methodology

Single lag X correlator in Simulink
Reconfigurable Open Architecture Computing Hardware (ROACH)
ROACH-based single FPGA test bed

- CASPER ROACH board, instrumented for accurate automated measurements of rail current
- Second ROACH generates test vector stimulus
- Need to isolate power consumed by FPGA design alone
- Look for step change on design loading and then enabling
- Evaluate sensitivity to clock rate, demux factor, architecture, number of baselines, etc
Power Consumption For 16- baseline XF Correlator

- Monitor power consumption of all inputs to FPGA
- Establish baseline power with FPGA suspended
- Enable correlator (at 11 seconds) and record power
- In this example, about 3.7 W for 16 baselines
CASPER FFT does not provide an independent enable line.

Power step about 1.8W 15/16 capability almost 1/2 power.
CASPER Packetized Correlator

F engines linked to X engines with 10GigE Switch

*Complex multiply allows for fine delay control and per-channel digital gain control. While coloured blocks not yet implemented.*
Year 2 Goals

- Investigate FX vs XF for large-N designs
- Optimize demux ratio, trading clock rate vs. FPGA design size
- Optimize single chip design (bit width, dump time, multiplier/adder implementation, …) w.r.t. power consumption
- Produce predictions of power, mass, volume requirements as a function of bandwidth and number of baselines
- Outline candidate architecture for LRA using multiple processors and required interconnects
Discussion

- Specific requests for trade studies?
- Is there a need for a functioning correlator for existing projects, e.g. ROLLS prototype testing, CubeSat?